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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/651,159	08/30/2000	Ole Bentz	MTI-31072	2115

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ART UNIT	PAPER NUMBER
2193	

DATE MAILED: 05/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/651,159	BENTZ, OLE	
	Examiner	Art Unit	
	Chat C. Do	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *4,5 and 10-12* is/are allowed.

6)☒ Claim(s) *1-3,6-8 and 13-20* is/are rejected.

7)☒ Claim(s) *9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 August 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is responsive to Amendment, filed 03/17/2005.

2. Claims 1-20 are pending in this application. Claims 1-4, 6-7, 13, and 15 are independent claims. This Office action is made final.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitation in claim 9 "**logically inverted prior** to the logically ORing" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will

be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-2, 6-8, 13-15, and 17-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Otaguro (U.S. 5,539,685).

Re claim 1, Otaguro discloses in Figure 10 a method of detecting overflow in a clamping circuit (abstract) comprising the steps of inputting a first operand having a first fixed point format (e.g. operand in 103 and col. 9 lines 25-26) into the clamping circuit; inputting a second operand having a second fixed point format (e.g. operand in 101 and col. 9 lines 14-15) into the clamping circuit; determining an overflow output (e.g. 108 and 109 in 107 of Figure 10) based upon the first and second fixed point format (inputs into 108 and 109 from 101 and 103 respectively) and predicting whether an arithmetic operation of the first operand with the second operand will yield a result that exceeds the overflow output (107); and performing at least partially the arithmetic operation of the first and second operands (106 for summing or accumulating all the partial products terms); wherein the determining and predicting step occurs independent from and substantially in parallel with the performing step (computation of 108 and 109 does not

require any parameters from the multiplier {104, 105, and 106}, therefore it is independent and substantially parallel).

Re claim 2, it has the same limitations as cited in claim 1 wherein Otaguro clearly discloses in Figure 10 and abstract that the arithmetic operation is a multiplier or a multiplication process. Thus, claim 2 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 6, Otaguro discloses in Figure 10 a method of processing multiplier data paths (abstract) comprising the steps of performing at least a partial multiplication of a plurality of operands (as seen in Figure 10 the overflow is checked or determined in every addition operation of the multiplication), each having a fixed-point format (103 and 101); determining whether the at least partial multiplication of the operands produces a product that will exceed a predetermined limit based upon the fixed-point format of each of the operands (107); and wherein the performance step and the determining step occur independently and substantially in parallel (computation of 108 and 109 does not require any parameters from the multiplier {104, 105, and 106}, therefore it is independent and substantially parallel).

Re claim 7, Otaguro discloses in Figure 10 a method of clamp detection (abstract) comprising the steps of inputting a first (103) and a second operand (101) to both a multiplier (104, 105, and 106 and abstract) and an overflow detection circuit (107); multiplying the first and second operands to generate a result not to exceed a predetermined number of bits (OVF); determining an initial clamping predictor bit (output of 109) based upon the first operand and the second operand (101 and 103); and

logically ORing (110) the initial clamping predictor bit and a most significant bit of the result to produce a final clamping predictor bit (110); wherein the multiplying and determining steps occur independently and substantially in parallel (computation of 108 and 109 does not require any parameters from the multiplier {104, 105, and 106}, therefore it is independent and substantially parallel).

Re claim 8, Otaguro further discloses in Figure 10 the first and second operands are in a fixed-point format (101 and 103).

Re claim 13, Otaguro discloses in Figure 10 a multiplication overflow detection circuit (abstract) comprising: multiplication circuitry for at least partially multiplying a first and a second operand (as seen in Figure 10 the overflow is checked or determined in every addition operation of the multiplication); and overflow detection circuitry (107) receiving the first and second operands that detects whether a result of the multiplication of the first and second operands exceed a maximum representable positive or negative value; wherein the multiplication circuitry and the overflow detection circuitry operate independently and substantially in parallel (computation of 108 and 109 does not require any parameters from the multiplier {104, 105, and 106}, therefore it is independent and substantially parallel).

Re claim 14, Otaguro further discloses in Figure 10 the overflow detection circuitry utilizes a fixed-point format of the first and second operands to determine whether the result of the multiplication exceeds the maximum representable positive or negative value (107).

Re claim 15, Otaguro discloses in Figure 10 an overflow detection circuit (abstract) comprising: a first register for storing a first operand (101); a second register for storing a second operand (103); overflow detection circuitry (108-109 and 110) for detecting an overflow of a multiplication of the first operand and the second operand and producing a clamp bit (output of 109); a multiplier (104, 105, and 106) for at least partially multiplying the fast and second operands and generating a result not to exceed a predetermined number of bits; a clamp bit register (col. 7 lines 24-25) for storing the clamp bit from the overflow detection circuitry; and a result register connected to the multiplier for storing the result of the multiplication of the first and second operands; wherein the overflow detection circuitry and the multiplier operate independently and substantially in parallel (computation of 108 and 109 does not require any parameters from the multiplier {104, 105, and 106}, therefore it is independent and substantially parallel).

Re claim 17, Otaguro further discloses in Figure 10 in addition to claim 15 the clamp bit input (output of 109) is logically ORed (110) with a most significant bit of the result (CARRY bit from adder to 110) stored in the result register.

Re claim 18, Otaguro further discloses in Figure 10 one of the registers is a flip-flop (101 and 103).

Re claim 19, it has same limitations cited in claim 8. Thus, claim 19 is also rejected under the same rationale as cited in the rejection of rejected claim 8.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 3, 16, and 20 are rejected under 35 U.S.C. 103(a) as being obvious over Otaguro (5,539,685) in view of Bonnet et al. (U.S. 6,321,248).

Re claim 3, Otaguro discloses in Figure 10 a method of clamping fixed-point multipliers (abtract) comprising the steps of providing a first operand in a first fixed-point format (103); providing a second operand in a second fixed-point format (101); at least partially multiplying the first operand with the second operand to produce an operation result (output of adder or accumulator in 106); determining whether the operation result will exceed a representable value (output of 107); wherein the multiplying step and determining whether the operation result will exceed the representable value step occur independently end substantially in parallel (computation of 108 and 109 does not require any parameters from the multiplier {104, 105, and 106}, therefore it is independent and substantially parallel). Otaguro does not disclose in Figure 10 a determining a clamping value based on the first fixed-point format of the fast operand and the second fixed-point format of the second operand (output of 109); and substituting the operation result with the clamping value when it is determined that the operation result will exceed the representable value. However, Bonnet et al. disclose in Figure 1 a determining a clamping value based on the first fixed-point format of the fast operand and the second

fixed-point format of the second operand (VALSAT* and VALSAT into 2); and substituting the operation result with the clamping value when it is determined that the operation result will exceed the representable value (by multiplexer in 2 into accumulator 3). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add a determining a clamping value based on the first fixed-point format of the fast operand and the second fixed-point format of the second operand (output of 109); and substituting the operation result with the clamping value when it is determined that the operation result will exceed the representable value as seen in Bonnet et al.'s invention into Otaguro's invention because it would enable to avoid compute incorrectly whenever overflow is encountered.

Re claim 16, it has same limitations cited in claim 15. In addition, Otaguro discloses the overflow detection circuit (abstract) comprising: a clamp value input for receiving a clamp value to be output when clamping occurs (107); a clamp bit register input (col. 7 lines 24-25) connected to the clamp bit register for receiving the clamp bit; a result register input, connected to the result register for receiving the result of the multiplication of the first and second operands (col. 7 lines 31-32). Otaguro does not disclose the overflow detection circuit comprising: a multiplexer comprising: an output wherein the multiplexer select one of the clamp value register input and the result register input based upon a logical level of the clamp bit register in order to make the selected input the output of the multiplexer. However, Bonnet et al. disclose in Figure 1 a multiplexer (2) comprising: an output wherein the multiplexer (input into 3) select one of the clamp value register input (VALSAT) and the result register input (S) based upon a

logical level of the clamp bit register (from 4) in order to make the selected input the output of the multiplexer. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add a multiplexer (2) comprising: an output wherein the multiplexer (input into 3) select one of the clamp value register input (VALSAT) and the result register input (S) based upon a logical level of the clamp bit register (from 4) in order to make the selected input the output of the multiplexer as seen in Bonnet et al.'s invention into Otaguro's invention because it would enable to avoid compute incorrectly whenever overflow is encountered.

Re claim 20, Otaguro discloses in Figure 10 a step of determining whether clamping occurs based upon g a logical value of the final clamping predictor bit (107). Otaguro does not disclose selecting one of a pre-selected clamp value and the result of the multiplying step. However, Bonnet et al. disclose in Figure 1 a determining a clamping value based on the first fixed-point format of the fast operand and the second fixed-point format of the second operand (VALSAT* and VALSAT into 2); and substituting the operation result with the clamping value when it is determined that the operation result will exceed the representable value (by multiplexer in 2 into accumulator 3). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add a determining a clamping value based on the first fixed-point format of the fast operand and the second fixed-point format of the second operand (output of 109); and substituting the operation result with the clamping value when it is determined that the operation result will exceed the representable value as seen

in Bonnet et al.'s invention into Otaguro's invention because it would enable to avoid compute incorrectly whenever overflow is encountered.

Allowable Subject Matter

8. Claim 9 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. Claims 4-5 and 10-12 are allowed.

Response to Arguments

10. Applicant's arguments filed 03/17/2005 have been fully considered but they are not persuasive.

a. The applicant argued in pages 12-14 for claims 1-2, 6-8, 13-15, and 17-19 that the cited reference by Otaguro does not disclose the first and second operands as fixed-point formats; a partial ALU calculations, and processing independently and parallel substantially as cited in the claimed invention.

The examiner respectfully submits that the primary reference by Otaguro does directly and indirectly disclose the first and second operands as fixed-point formats; a partial ALU calculations, and processing independently and parallel substantially. First, the reference does not limit the first and second operands to any particular operand format and the circuit structure does not require any particular operand format either. Therefore, the examiner interprets the first and

second operands format as fixed-point formats since they are properly function with the circuit. Second, Figure 10 clearly discloses the partial ALU calculations as the adder 106. This adder in repetitive would act as an accumulator wherein it would add or sum all the inputs operands from 104 and 105. Third, Figure 10 can be seen and interpreted the adder operation (e.g. 106) and the overflow/claimping (e.g. 107) detection processing in parallel and independently. Wherein the overflow/claimping detection comprising two parts: first part including 108 and 109 for yielding an overflow prediction and the second part including OR logic gate 110 for yielding an actual overflow signal. Therefore, the first part of the overflow/claimping detection can process independently and in parallel with the adder 106.

b. The applicant argued in pages 15-17 for claims 3, 16, and 20 that first Bonnet's reference is applied incorrectly because the VALSAT* and VALSAT are not the first and second operands respectively, second Otaguro's reference does not disclose a step of receiving a clamp value to be output when clamping occurs, and third Otaguro's reference does not disclose a logical value of the final clamping predictor bit as cited in claimed invention.

First, the examiner had never interpret or cited the VALSAT* and VALSAT as the first and second operands respectively in Bonnet's reference. The examiner interprets the VALSAT* and VALSAT as clamped values or saturated values in Bonnet's reference. Second, Otaguro's reference discloses a step of receiving a

clamp value to be output when clamping occurs (e.g. 107). Third, the logical value of the final clamping predictor bit is the output of OR logic gate 110.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

c. U.S. Patent No. 6,535,900 to Perets et al. disclose an accumulation saturation by means of feedback.

d. U.S. Patent No. 5,745,393 to Wong discloses a left-shifting an integer operand and providing a clamped integer result.

e. U.S. Patent No. 5,844,827 to Wong discloses an arithmetic shifter that performs multiply/divide by two to the NTH power for positive and negative N.

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on 7:00AM to 5:00PM M-Th.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (571) 272-3719. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C Do
Examiner
Art Unit 2193

April 22, 2005

TODD INGBERG
PRIMARY EXAMINER